2000V 45mΩ SiC MOSFET Bare Die
QS45SCM200X62

Product Overview

The QS45SCM200X62 is a high-voltage 2nd Generation silicon carbide MOSFET supplied in bare die form, designed for high-efficiency, high-frequency power conversion. Its 2000V blocking voltage, low on-resistance, robust intrinsic body diode, and 175°C junction temperature capability support demanding industrial, solar, and power-supply applications.

Features

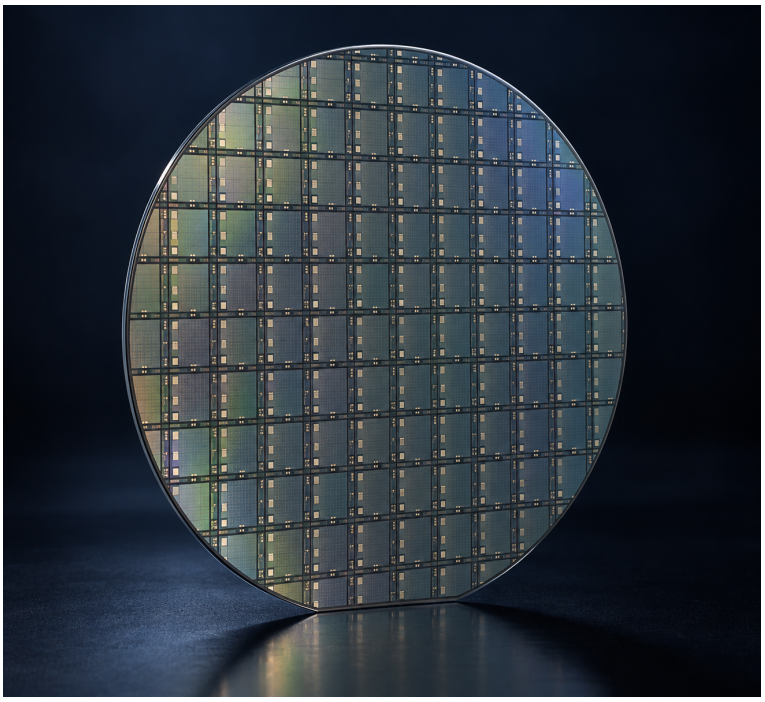
- 2nd Generation SiC MOSFET Technology with +15~+18V gate drive
- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- 175°C operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design
- Bare die format: suitable for custom packaging and direct die attach

Applications

- Solar boosters
- UPS power supplies
- Motor drivers
- Switch mode power supplies
- High voltage DC-DC converters

Part Number Information

Part Number	Description	Package
QS45SCM200X62	2000V 45mΩ SiC MOSFET Bare Die	Die (BD suffix)



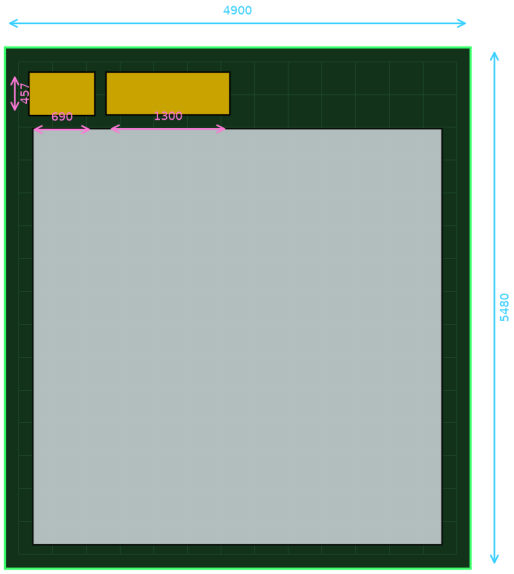
Absolute Maximum Ratings

TC=25°C unless otherwise specified

Symbol	Parameter	Value	Unit	Test Conditions	Note
Vds	Drain-Source voltage	2000	V	Vgs=0V, Id=100μA	
Vgsmax (Transient)	Maximum transient voltage	-10 to 23	V	Duty cycle<1%, and pulse width<200ns	
Vgson	Recommended turn-on voltage	15 to 18	V		
Vgsoff	Recommended turn-off voltage	-5 to -2	V	Typical -3.5V	
Id	Drain current (continuous)	62	A	Vgs=18V, Tc=25°C	Fig.23
Idc	Drain current (continuous)	46	A	Vgs=18V, Tc=100°C	Fig.23
Idm	Drain current (pulsed)	155	A	Pulse width limited by SOA and dynamic Rθ(j-c)	Fig.25,26
Ism	Body diode current (pulsed)	155	A	Pulse width limited by SOA and dynamic Rθ(j-c)	Fig.25,26
Ptot	Total power dissipation	500	W	Tc=25°C	Fig.24
Tstg	Storage temperature range	-55 to 175	°C		
Tj	Operating junction temperature	-55 to 175	°C		
Tl	Solder Temperature	260	°C	Wave soldering only allowed at leads, 1.6mm from case for 10s	

Note 1: Assumes Rθ(j-c) < 0.3°C/W.

Die Drawing



Chip size (W/O scribe line): 4900×5480μm

Chip size (With scribe line): 4980×5560μm

Gate Pad: 690×457μm

Kelvin Source Pad: 1300×450μm

*Die outline dimensions are engineering estimates; contact Quest Semiconductors sales for confirmed die-level metrology on a per-lot basis.

Mechanical Parameters

Parameter	Typ.	Unit
Die Size	4900 × 5480	μm²
Source Pad Size (L×W)	3900 × 4400	μm²
Kelvin Pad Size (L×W)	1300 × 450	μm²
Gate Pad Size (L×W)	690 × 457	μm²
Thickness	180 ± 20	μm
Wafer Size	150	mm
Top Side Source Metallization (AlCu)	4	μm
Top Side Gate Metallization (AlCu)	4	μm
Bottom Drain Metallization (Ti/Ni/Ag)	0.2 / 0.2 / 1	μm
Frontside Passivation (Polyimide)	5	μm

*Mechanical parameter values above are representative engineering estimates based on the device electrical rating class; the source specification did not publish die-level mechanical data for this part.

Electrical Characteristics

TC=25°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
Idss	Zero gate voltage drain current		1	10	μA	Vds=2000V, Vgs=0V	
Igss	Gate leakage current			±100	nA	Vds=0V, Vgs=-5~20V	
Vth	Gate threshold voltage	1.8	2.8	4.5	V	Vgs=Vds, Id=10mA	Fig.8,9
Vth	Gate threshold voltage		2.2		V	Vgs=Vds, Id=10mA @Tj=175°C	
Ron	Static drain-source on-resistance		43	56	mΩ	VGS=18V, ID=20A @Tj=25°C	Fig.4,5,6,7
Ron	Static drain-source on-resistance		105		mΩ	Vgs=18V, Id=20A @Tj=175°C	
Ron	Static drain-source on-resistance		48		mΩ	Vgs=15V, Id=20A @Tj=25°C	
Ron	Static drain-source on-resistance		110		mΩ	Vgs=15V, Id=20A @Tj=175°C	
Ciss	Input capacitance		3950		pF	Vds=1500V, Vgs=0V, f=1MHz	Fig.16
Coss	Output capacitance		110		pF		
Crss	Reverse transfer capacitance		13		pF		
Eoss	Coss stored energy		145		μJ		Fig.17
Qg	Total gate charge		175		nC	Vds=1500V, Id=20A, Vgs=-3 to 18V	Fig.18
Qgs	Gate-source charge		43		nC		
Qgd	Gate-drain charge		63		nC		
Rg	Gate input resistance		1.5		Ω	f=1MHz	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
Eon	Turn-on switching energy		870		µJ	Vds=1200V, Id=20A, Vgs=-3.5 to 18V, Rg(ext)=3.3Ω, L=400µH, Tj=25°C	Fig.19,20
Eoff	Turn-off switching energy		150		µJ		
td(on)	Turn-on delay time		25		ns		
tr	Rise time		24		ns		
td(off)	Turn-off delay time		40		ns		
tf	Fall time		23		ns		

Reverse Diode Characteristics

TC=25°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
Vsd	Diode forward voltage		3.5		V	Isd=20A, Vgs=0V	Fig.10,11, 12
Vsd	Diode forward voltage		3.4		V	Isd=20A, Vgs=0V, Tj=175°C	
trr	Reverse recovery time		46		ns	Vgs=-3.5V/+18V, Isd=20A, Vr=1200V, Rg(ext)=5.1Ω, di/dt=3000A/µs	
Qrr	Reverse recovery charge		550		nC		
Irrm	Peak reverse recovery current		23		A		

Typical Performance Curves

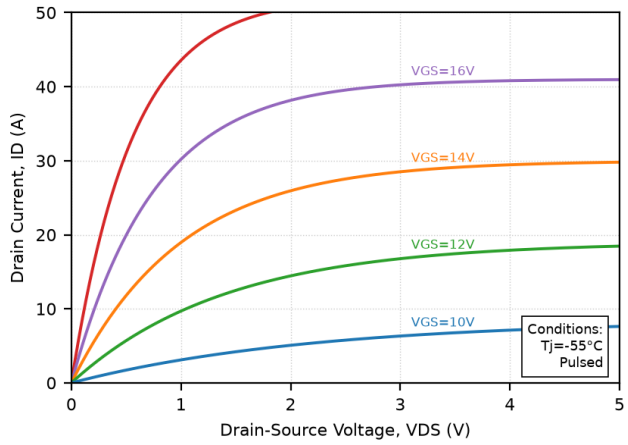


Fig. 1 — Output Curve @ Tj=-55°C

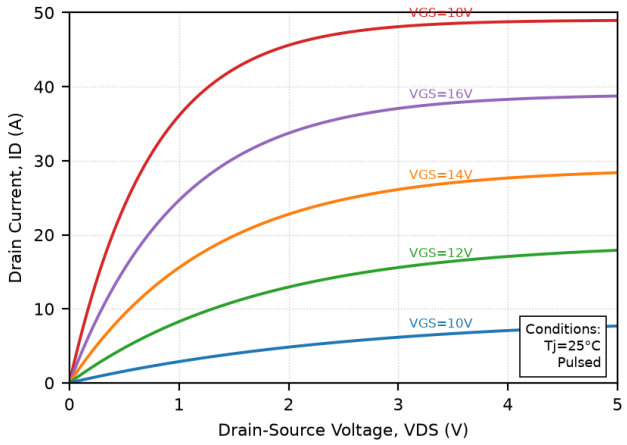


Fig. 2 — Output Curve @ Tj=25°C

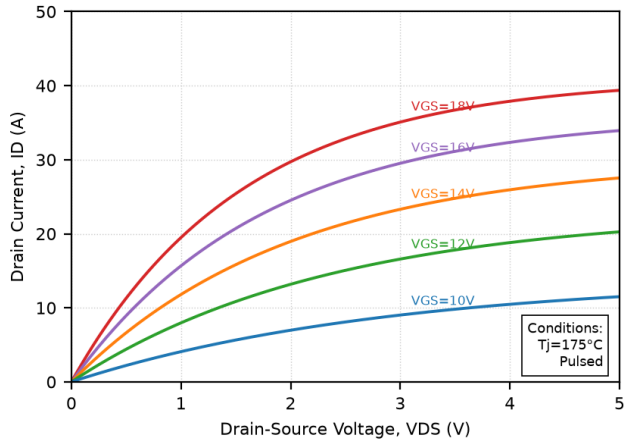


Fig. 3 — Output Curve @ Tj=175°C

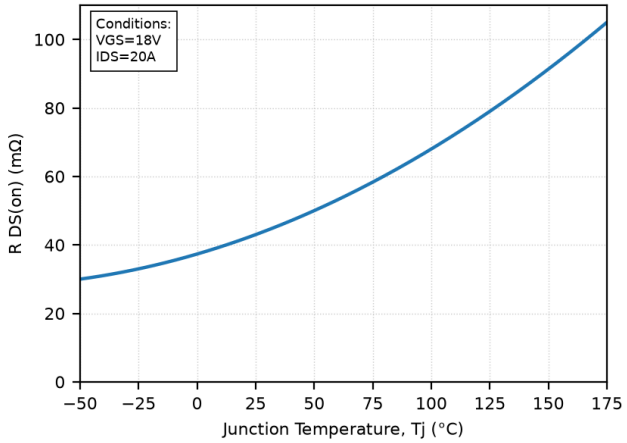


Fig. 4 — R DS(on) vs. Junction Temperature

Typical Performance Curves

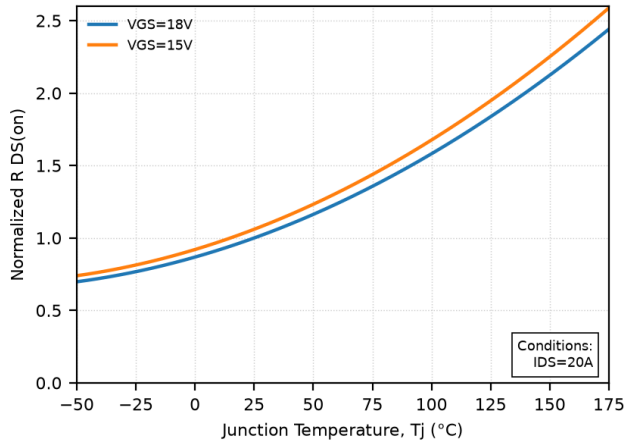


Fig. 5 — Normalized R DS(on) vs. Junction Temp

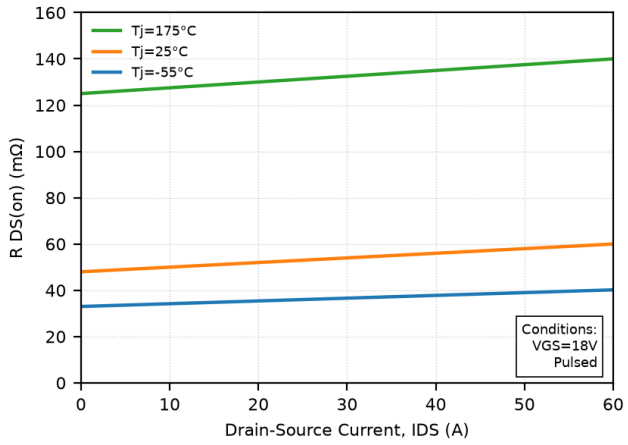


Fig. 6 — R DS(on) vs. IDS @ Various Temperature

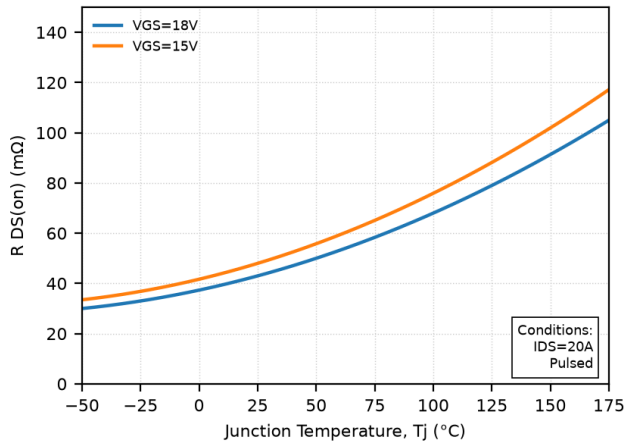


Fig. 7 — R DS(on) vs. Temperature @ Various VGS

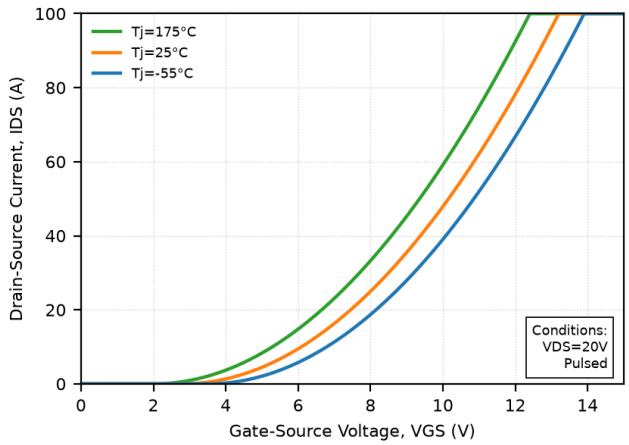


Fig. 8 — Transfer Curves @ Various Temperature

Typical Performance Curves

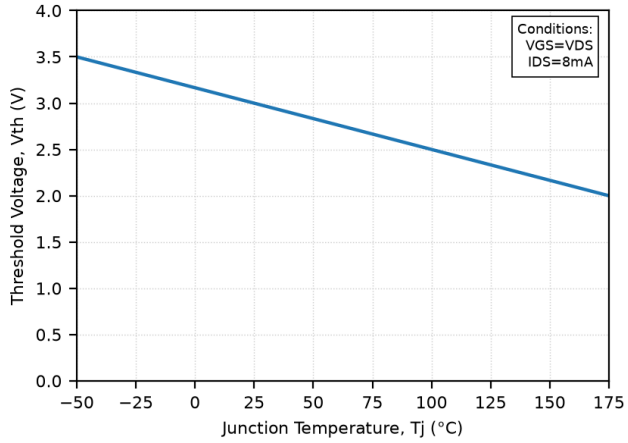


Fig. 9 — Vth vs. Junction Temperature

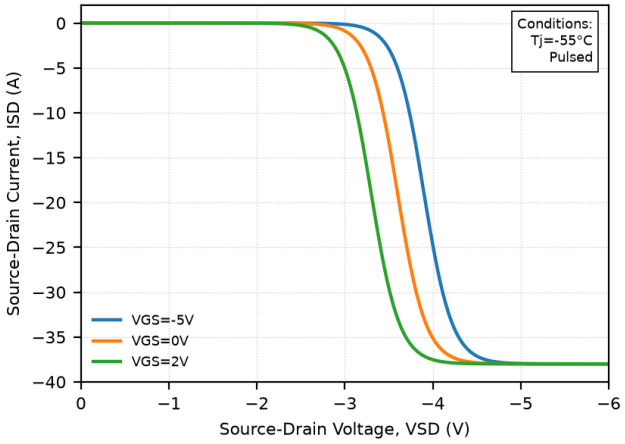


Fig. 10 — Body Diode I-V @ Tj=-55°C

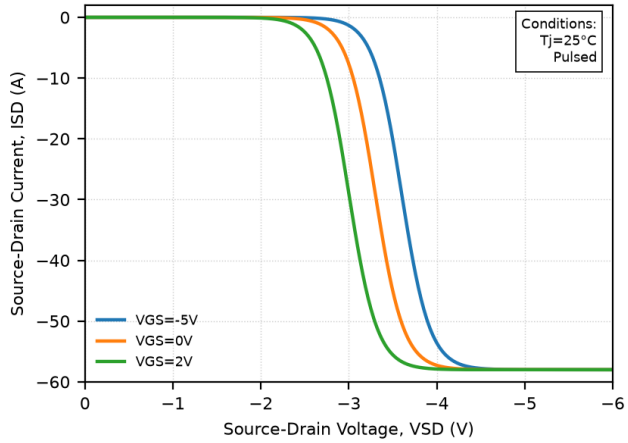


Fig. 11 — Body Diode I-V @ Tj=25°C

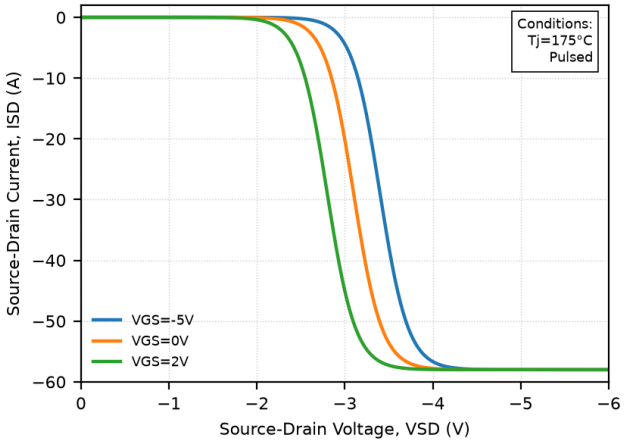


Fig. 12 — Body Diode I-V @ Tj=175°C